IN THE CLAIMS

After adding claims 26-37 as provided below, please cancel claims 1-25 without prejudice or disclaimer.

Sub E1 A3

26. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

27. [New] The system of claim 26, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

28. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

29. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

30. [New] The system of claim 29, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

31. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

32. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device having a first operation mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the first operation mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

33. [New] The system of claim 32, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

34. [New] A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device having a first operation mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the first operation mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

35. [New] A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst access memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the